High Energy Backscattered Electron Imaging of Subsurface Cu Interconnects

Lynne M. Gignac¹, Masahiro Kawasaki², Steven H. Boettcher³ and Oliver C. Wells⁴

¹IBM T. J. Watson Research Center
²JEOL USA, Inc.
³IBM Microelectronics Division
⁴IBM T. J. Watson Research Center, Emeritus

In bulk Si integrated circuit devices, passivated copper interconnects that were located 0.65-2.7 µm below the surface were imaged in two different transmission electron microscopes with scanning attachments by detecting backscattered electrons (BSEs) using incident beam energies that ranged from 150 keV to 400 keV. Since the BSE yield was strongly dependent on atomic number, voids in the subsurface Cu interconnects could be detected without having to alter the sample by cross-sectioning or delaying even when the voids were located under complex, dielectric surface topography or upper level Cu lines or vias. Because the electron beam broadens from low angle, elastic scattering events during the initial stages of penetration into the sample, the subsurface image resolution depended on the depth below the surface where the electrons were backscattered, the composition of the overlying material, and the incident beam energy. Beam spreads were measured at several beam energies from BSE images of Cu interconnects buried under varying thicknesses of SiO₂-SiNx dielectric. Tilt series tomography was attempted on passivated, 2-level Cu interconnects but increased beam spread and decreased signal with tilt allowed imaging up to only ±40°.

**Introduction**

The scanning electron microscope (SEM) is a critical tool for in-line defect characterization, critical dimension measurements and failure analysis of semiconductor devices. As devices continue to shrink, the trend in imaging fine semiconductor structures in the SEM has been to use field emission electron sources at low beam energies, < 5 keV, and to detect secondary electrons (SE). This small spot, low beam current configuration can produce high resolution images of the sample surface with minimal sample charging. However, when higher energy incident electron beams are employed and backscattered electrons (BSEs) are detected, images can be obtained with high topographic or atomic number (Z) contrast and detail below the sample surface can be detected [1-5]. A specific application for BSE subsurface imaging is for the characterization of multi-level Cu interconnects passivated with SiO₂ or low dielectric constant amorphous dielectrics [6-22]. Here the low Z surface dielectric does not greatly scatter the electron beam allowing the higher Z, Cu-Ta containing subsurface lines to be imaged with BSEs. Defects such as voids in Cu interconnects or metal extruded out of the interconnect can be imaged with one, topdown BSE image even if the defect is buried under complex, dielectric surface topography or upper level metal. BSE imaging has potential as a technique that is able to characterize subsurface device structures without having to physically alter the sample by cross-sectioning or delaying though electron beam induced damage of devices has been reported [11-12].

Initial work on BSE subsurface imaging of interconnect structures was published in the 1990’s where both SEMs [6-8, 10-15] and transmission electron microscopes (TEMs) with scanning attachments [6, 9, 17] were used to image Al interconnects passivated with SiO₂ or SiNx. Since the image resolution was dependent on the beam spread caused by scattering by sample atoms, higher energy incident electron beams were used to reduce beam broadening and to improve the resolution of the BSE images.

Energy filtered BSE imaging has been studied as a microtomography technique where a series of images representing specific BSE energies were collected for a given incident electron beam energy [13-15]. Since BSEs which have lost a certain amount of energy are typically generated from a given depth in the sample, an energy-filtered image series represents two-dimensional slices of the sample at various points below the sample surface. Since interconnects are non-uniform in composition laterally, an energy-filtered image can suffer from contrast inversion where a low atomic number layer that is located deep below the surface can have higher intensity than a high atomic number layer located closer to the surface. Therefore, a given BSE energy image will represent a variety of depths below the surface making the microtomography reconstruction difficult.

In recent years, there has been renewed interest in using BSE to image subsurface interconnect structures [18-21]. In this paper, subsurface imaging of multi-level Cu interconnects with BSEs is demonstrated by using transmission electron microscopes with scanning attachments with beam energies of 150 keV to 400 keV. The BSE images were used to detect voids in subsurface Cu interconnects and to characterize beam spread at various depths below the surface.

**Experimental Procedure**

High voltage BSE imaging of bulk, passivated Cu-SiO₂-SiNx, interconnects was performed at 150 keV and 400 keV using a JEOL JEM-4000FX TEM with a LaB₆ thermionic source and at 300 keV in a JEOL JEM-3000F TEM with a Schottky field emission source. Both TEMs were equipped with scanning attachments and BSE detectors. The JEM-4000FX had a rectangular shaped, 2-piece Si solid state BSE detector located under the objective polepiece, 4 mm above the sample surface with a hole in the center to allow passage of the electron beam. The detector solid angle was ~1.3 sr and it detected electrons backscattered at angles of 27-54° from the incident beam direction. The JEM-3000F had a microchannel plate (MCP), annular shaped, center hole detector located above the objective polepiece, 46 mm above the sample surface. The detector solid angle was ~0.14 sr and it detected electrons backscattered at angles of 3-12° from the incident beam direction. The MCP detector could be biased allowing the detection of either BSEs or SEs. In addition to the solid state BSE detector, the JEM-4000FX had an Everhart-Thorley SE detector.
Bulk samples could be inserted in both microscopes using standard sample holders if they were cored into 3 mm discs and backside polished to reduce the sample thickness. In the JEM-4000FX, a bulk specimen holder was also available and could be used to study chips that had dimensions less than 4 × 8 mm. In both microscopes, electronic BSE images could be acquired using digital image capture systems.

Free lens control was used to create higher current probes than the standard probes used for scanning transmission electron microscope (STEM) bright field or dark field imaging of thin samples. The high current conditions were produced by weakening the first condenser lens strength so that a larger sized probe was formed with increased total current. A Faraday cup was not available to measure the probe current in the JEM-4000FX but a value of ~13 nA was estimated for the free lens generated BSE probe. For the JEM-3000F, a Faraday cup measured the high current probe to be 10 nA; a current ~20 times greater than the standard 1 nm STEM probe.

Various multilevel, passivated Cu interconnects were studied in this work. All samples were produced using Cu single or dual Damascene processing [22] where a blanket dielectric layer was initially deposited on the wafer. Lines and vias were patterned in the dielectric using photolithography and reactive ion etching and then metal was deposited to fill the open lines and vias. Chemical-mechanical polishing (CMP) was used to remove the excess metal and to planarize the layer. The deposited metal layers consisted of a thin, sputtered deposited TaN/Ta liner [23] followed by a sputtered Cu seed layer and then electroplated Cu. The dielectric material consisted primarily of SiO₂ but all Cu levels were capped with a thin SiNₓ film. All samples were passivated with dielectric so that the Cu interconnects were located below the sample surface. The samples contained between 1-3 Cu levels.

Results and Discussion

When the high voltage BSE imaging technique was initially being developed in the JEM-4000FX, a standard “L” STEM probe was selected that was typically used for bright field imaging of thin samples. In Fig. 1a, a TEM micrograph of a two-level Cu interconnect is shown in cross-section where the top M2 Cu line is located under 0.65 µm of SiO₂/SiNₓ dielectric, the lower M1 Cu line is located 1.60 µm below the surface and an Al bond pad is seen on the dielectric surface. In Fig. 1b, a low magnification BSE image of this 2-level Cu interconnect structure is seen at 400 keV with a standard JEM-4000FX “L” STEM probe. Though an image was obtained showing the Al bond pad and the subsurface M2 and M1 Cu levels, the image was very noisy and not very informative. When free lens control was used to generate a higher incident beam current, a sharper BSE image was obtained with significantly lower noise, see Fig. 1c. The sample studied in Fig. 1 was produced using a non-standard processing condition that caused a high density of stress voids to be produced in the Cu conductors. These voids are seen as regions of dark contrast in both the M2 and M1 Cu lines in Fig. 1c.

In Fig. 1c, the sensitivity of BSE imaging to atomic number (Z) contrast is shown not only in large signal intensity differences between the voided and non-voided regions in the Cu lines but also by the intensity differences in areas with TaN/Ta liner, Cu, and SiO₂/SiNₓ dielectric. Since previous studies have shown that the BSE signal intensity can be directly related to the thickness of a single thin film, [4-5, 24-25] the signal intensity in the Cu line regions of the BSE image can be related to the amount of Cu in that region. The M2 and M1 Cu conductors were both 0.35 µm thick and the individual M2 and M1 regions had similar signal intensity levels in Fig. 1c. The M2/M1 overlap regions had much greater signal intensity than the individual layers. Though multilevel Cu interconnect samples are more complex than single layer films, BSE imaging, with the aid of Monte Carlo simulations and sophisticated image analysis routines, could be developed as a quantitative analytical technique where void volume or film thickness could be measured from a single BSE image without having to cross-section the sample.

Fig. 2 shows TEM and BSE images of a 3-level Cu electromigration (EM) test structure. Fig. 2a is a TEM cross-section image of the anode end of an untested structure showing an upper M3 Cu level under 0.65 µm of SiO₂/SiNₓ, a middle level M2 Cu electromigration test structure 1.75 µm below the surface, and a M1 Cu fill structure 2.70 µm below the surface. A V2 Cu via connects the M3 line to the M2 test structure. In Figs. 2b and 2c, BSE images of the anode end of a stressed electromigration test structure are shown at 150 keV and 400 keV. All three Cu levels are seen in both images, even the lowest level M1 fill structure. There is a large void in the top level M3 line near the V2 contact and this void was imaged with greater contrast at 150 keV than at 400 keV. In both BSE images, the edges of...
the M3 lines have a band of brighter intensity due to Z contrast from the fine TaN/Ta liner that encased the Cu lines. The edges of all the lines are sharper at 400 keV than at 150 keV showing that the subsurface 400 keV BSE image had better resolution. During the initial stages of penetration into the sample, the beam spreads due to small angle Rutherford scattering while intensity is lost from that compact part of the beam from wide angle Rutherford scattering events. At a given depth, a 400 keV electron beam will be narrower than a 150 keV beam and will produce a better resolution, subsurface BSE image. However, the 400 keV electron beam will penetrate deeper into the sample than the 150 keV beam and will generate fewer BSEs in the upper layers. Thus, the Z contrast generated by the void in the M3 layer was less at 400 keV than 150 keV [4].

The ability to detect Z contrast from the TaN/Ta liner was dependent on the liner thickness and the beam spread. The beam diameter varied depending on the incident electron energy, the overlayer material and the depth below the surface where the structure was located. The beam diameter at various depths below the surface after passing through SiO₂-SiNₓ dielectric was measured from BSE images taken at 30 keV, 150 keV and 400 keV by taking an intensity line scan across the edge of wide Cu lines where the intensity changed from a low signal in the SiO₂-SiNₓ dielectric to a high signal in the Cu line. The 30 keV data was obtained from BSE images taken on a cold field emission SEM. The derivative of the line scan was plotted and the beam diameter was estimated from the full-width half maximum (FWHM) of the derivative peak. When there was TaN/Ta-Cu Z contrast, the beam diameter was calculated as twice the half-width at full maximum where the half-width was taken from the side of the derivative peak going from dielectric to TaN/Ta.

In Fig. 3, the measured values of the beam diameters (solid symbols) are plotted versus the dielectric overlayer thickness. A least squares fit to the measured data is shown as dashed lines. For comparison, a theoretical estimate of the beam spread is given as solid lines. The theoretical values were obtained by using Goldstein et al.’s [26] beam broadening relation for a single Rutherford scattering event through SiO₂. The theoretical and experimentally determined subsurface beam diameters agreed for overlayer thicknesses less than 0.65 µm. As the SiO₂ overlayer thickness increased, the measured diameters were less than the theoretical values and, for 150 keV, the beam spread began to levels off at SiO₂ overlayer thicknesses greater than 2 µm. Even though the Goldstein et al. relation was derived from a single electron scattering event and these BSE images resulted from multiple scattering events, the experimentally derived diameters were less than the measured diameters. The leveling off of the beam spread with

![Fig. 2 Anode end of a passivated, 3-level electromigration test structure: a) TEM cross-section micrograph of an unstressed structure and BSE images of a stressed structure taken at b) 150 and c) 400 keV, respectively.](image)

![Fig. 3 A plot of beam spread versus SiO₂ overlayer thickness: symbols are measured values, dotted lines are least squares fits to the measured data and solid lines are theoretical predictions of the beam spread.](image)
thick overlayers was predicted from Monte Carlo simulations by Rau and Reimer [18]. Their simulations showed that an incident electron could not deviate greatly from the incident beam position to be able to make it to a great depth below the surface and at that depth, the electron had equal probability of making it out of the sample or being absorbed. Thus, at large depths, the actual beam spread was less than theoretical predictions. It may be difficult to take advantage of the reduced beam spread at great depths below the surface because the detectable BSE signal also decreases with depth.

In the BSE images in Figs. 2b-c, TaN/Ta-Cu Z contrast is seen for the top M3 Cu level at both 150 keV and 400 keV. The M3 level was located 0.65 µm below the sample surface and the liner sidewall thickness varied from 0.05 to 0.08 µm. From Fig. 3, it is expected that the high energy incident electron beams would produce TaN/Ta-Cu Z contrast since the beam diameter was 0.05 µm and 0.03 µm at 150 keV and 400 keV. Here the beam size was less than or equal to the liner thickness. At 30 keV, the beam spread to 0.24 µm at M3 level and, in the SEM BSE image, no liner-Cu Z contrast was observed. In Figs. 2b-c, liner-Cu Z contrast was not seen at the M2 level for 150 keV and 400 keV but was just barely distinguished at the M1 level for 400 keV only. Previous studies have shown that TaN/Ta to Cu Z contrast is seen when the beam diameter is ≤ 1.5 times the liner thickness [20].

BSE imaging can be used to image voids in Cu lines below complex, dielectric surface topography. Damascene interconnect processing involves creating open trenches and vias in dielectric and then filling the open regions with TaN/Ta and Cu metals. The vias connect one metal level to another and there can be 9 or more Cu levels in advanced chips. When there is a problem with voiding in an existing Cu line when processing the next metal level, a complex surface structure of open trenches and vias can obscure the imaging of the lower level Cu. An example of this surface structure is shown in Fig. 4a where a 150 keV SE image of open dual Damascene M2 trenches and V1 vias is shown. In this sample, there is a Cu M1 level under the open V1 vias and the sample was subjected to a Cu etch solution to partially remove M1 Cu. Below the M1 Cu lines, there are tungsten CA vias that connect the M1 level to Si. In the SE image, the open M2 trenches and V1 vias are clearly seen along with some subsurface M1 Cu lines and CA W vias.

In Fig. 4b, a 150 keV BSE image of the same region shown in Fig. 4a is given and an ion-induced secondary electron cross-section image taken at 45° with a focused ion beam microscope is shown in Fig. 4c. The region of the chip that was sectioned is shown as dotted lines in Figs. 4a-b. The BSE image differed from the SE image in that the surface dielectric and open structures were not seen but the subsurface M1 lines and W CA vias were clearly distinguished. The SiO2-SiN4 dielectric was composed of low Z elements which did not produce many BSE. Thus, there was not much BSE signal intensity difference between full thickness dielectric regions and the open M2 trench regions.

In the BSE image in Fig. 4b, the voids that were intentionally produced by etching the M1 Cu were detected as dark regions in the M1 lines and the W CA vias were visible as bright round circles. These features can also be seen in the cross-section in Fig. 4c. It would be difficult to find voids in M1 lines under open M2/V1 structures by any other top-down imaging or inspection technique. A SE image would be confounded by the open surface structures and optical inspection methods would suffer from light scattering off these structures in addition to being limited by resolution when imaging sub-0.1 µm wide lines.

Since a high energy BSE image is a planar composite of multiple metal levels, BSE imaging could be used to verify the alignment on or inspect defects in various subsurface metal layers. However, it would be difficult to analyze very large regions on a chip since high energy BSE imaging must be done in a TEM that typically can only hold samples that are 3 mm diameter. It is not difficult to imagine the usefulness of a high energy SEM with a large sample stage that could be used for wafer inspection and failure analysis especially since defects such as voids in Cu lines can be detected without having to physically damage a wafer. However, development of this type of tool may be hindered by the fear of electron beam induced semiconductor device defects.

A final example of subsurface, high energy
BSE imaging is an attempt to do BSE tilt series tomography on the stress voided, 2-level Cu line shown in Fig. 1. The region of the chip that was imaged for tilt tomography contained a 5 µm wide M2 Cu line connected to a 5 µm wide M1 Cu line through a sea of V1 vias. This stress voided chip was a good initial candidate for tomography to be able to visualize the depth and location of the voids near vias. A BSE image of this region of the chip that was taken in the JEM-3000F field emission TEM at 300 keV is shown at 0° tilt in Fig. 5a. The intention of this experiment was to take a series of images at a range of tilts from ±70° and then use tomography software to construct three-dimensional representations. However, as the tilt increased, the beam traveled through increased sample thicknesses which caused the beam to broaden. In addition, the signal significantly decreased with tilt and images could only be recorded at maximum tilt values near ±40°, see Figs. 5b-c. At high tilts, BSE were forward scattered away from the fixed detector which was situated below the polepiece, 90° from the flat sample surface. BSE tilt series tomography initially seemed to be a good idea since minimal sample preparation was required and a large imaging volume could be sampled but the problems of beam spread and signal loss defeated this initial attempt. Improved BSE tilt tomography could probably be accomplished with a moveable or variable position BSE detector but typically there is limited space in a TEM polepiece.

Conclusions

BSE imaging of passivated Cu interconnect structures was used to image voids in Cu lines even when the lines were buried 1.6 µm below the surface or under complex, dielectric surface topography. The subsurface image resolution and TaN/Ta-Cu Z contrast were limited by the spreading of the beam that occurred from a small-angle scattering of the incident electron beam with atoms in the sample. The beam broadening was measured for various SiO2 surface layer thicknesses and incident beam energies. Tilt series BSE tomography was attempted but was not successful because the beam spread increased and the signal significantly decreased as the sample was tilted away from the fixed detector which was located below the objective polepiece. Commercial development of a SEM with both high incident beam energy and large sample stage capabilities could be beneficial to decreasing cost and increasing yield in a semiconductor fab since defect inspection and failure analysis could be performed on a full wafer without having to scrap the wafer. However, there are several deterrents that could hinder tool development which include beam spread and image resolution on the order of the sub-0.1 µm Cu line dimension, low dielectric constant dielectrics that shrink when imaged with an electron beam, increased fill structures at each Cu level that improves CMP uniformity but obstructs BSE subsurface imaging and electron beam induced semiconductor device defects.

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